Performance Comparison of Single and Dual Stage MMIC Limiters

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***Abstract* — This papers details a performance comparison between single and dual stage MMIC PIN Limiters. The two limiters were designed for the best 3 to 28 GHz small signal performance with minimum die size possible. The dual stage limiter was 32% larger than the single stage but provided many performance benefits. Simulations and measurements of the fabricated devices give insight into critical performance trade-offs valuable for future limiter design efforts.**

I. Introduction

Limiters perform an important function in RF systems by protecting power-sensitive components from damage or burnout. Limiters attenuate high power signals while exhibiting low loss at small signal levels. Most limiters are used in a receive path before a Low Noise amplifier and are therefore called Receive Protect (RP) Circuits. Microwave phased array antennas commonly use a RP for each antenna element to guard against excessive power being fed into the receive path usually by unintentional reflections of the power combined transmission path.

In most applications, a limiter must have the following characteristics:

1) Low small signal insertion loss
2) High Power Survivability
3) High Limiting for Large Input Powers
4) Small Size for low cost

These criteria can successfully be satisfied using a monolithic limiter implementation. GaAs PIN diodes are a particularly ideal choice since they have low-off state capacitance, small on-state resistance, high power handling capability, and are produced on a low loss substrate capable of supporting mm-wave frequencies.

II. VPIN Diodes Fabrication and Modeling

The PIN diode derives its name from the fact that it consists of an intrinsic region sandwiched between a heavily doped *p* and *n*-type semiconductor. Mobile charge carriers are injected into the I-region during forward bias, which rapidly changes the PIN diode from a low capacitance, high resistance active device to a high capacitance, low resistance state. This large parameter change can be taken advantage of by creating phase shift, attenuator, and limiter circuit functions [1,2].

Vertical PIN (VPIN) diodes are particularly ideal for circuit designs because they are highly compact, robust, and exhibit low off-state capacitance. Additionally, they are created monolithically with transmission lines, vias to ground, resistors, and MIM capacitors. TriQuint VPIN diodes are fabricated from a highly controlled MOCVD grown epitaxial GaAs wafer defined using optical lithography and etched in the vertical dimension using reactive ion etching [2,3]. VPIN diodes exhibit reverse breakdowns greater than 35V, forward bias resistance lower than 2 ohms, and off-state capacitances in the hundreds of femto-Farads range (depending on size). The highly controlled lithographic fabrication process creates circuits that are exceptionally consistent and exhibit very high DC and RF yields.

A common Linear PIN Intrinsic diode model is shown in Figure 1. The parameters R_i and C_i represent the resistance and capacitance of the Intrinsic (I) region. The R_D represents the conductance of the depletion region. C_D models both the junction and diffusion capacitance across the depletion region. R_S accounts for the contact resistance of the anode and cathode together with the total bulk resistance of the *p*- and *n*-layers. The intrinsic model can be combined with distributed feed models to successfully fit VPIN performance over bias, frequency, and various diodes sizes [4]. This modeling methodology was used to accurately fit VPIN electrical behavior 6 to 45GHz from reverses bias to the fully "on" diode state.

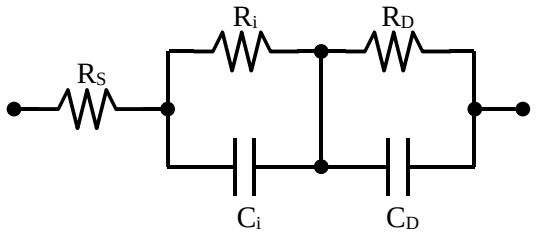

Figure 1: Intrinsic Linear PIN Diode Model

III. Limiter Design

Limiters are typically designed using the PIN diode shunt to ground configuration. A high power RF signal imposed across the PIN diode injects carriers into the I-region during the forward bias swing of the signal. This injection causes the capacitance of the diode to increase

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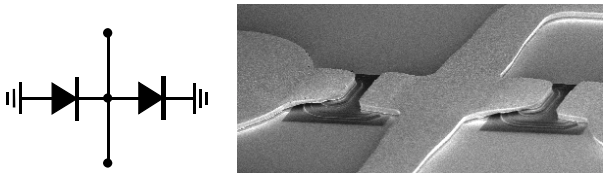
and resistance to decrease which in turn causes the diode impedance to drop dramatically. The higher the swing of the signal the more the electrical parameters change and the lower the diode impedance is driven. The low device impedance causes the incident signal to be reflected and therefore a lower percentage of the input signal will reach the output of the limiter. This causes the varying attenuation of input signal depending on the incident power level.

I-region carrier recombination from large incident signals requires that the designer provide a DC return path in the limiter [5]. The two approaches are with a RF choke shunt to ground or with a anti-parallel combination of diodes called a PIN-NIP pair shown in the Figure 2a Schematic [1]. A SEM of the monolithic implementation of the PIN-NIP Pair is shown in Figure 2b representing the "elongated" diode layout with through substrate via pads. The anti-parallel diodes provide the DC return when the transit time of the carriers though the I-region is longer than a half cycle. This occurs in VPIN diodes above about 80MHz [2]. The easier and least lossy of these two design approaches is the PIN-NIP pair since the RF Choke inductance increases small signal insertion loss at lower (<30GHz) frequencies.



(a) (b)

Figure 2: Schematic and SEM of a PIN-NIP Pair

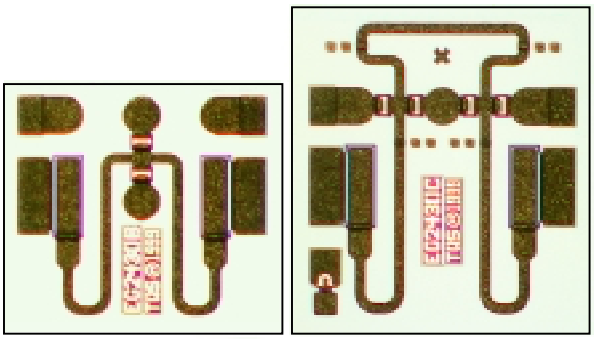
The limiting diodes represent a small, yet significant shunting capacitance to ground, which at microwave frequencies cause incident wave reflections at small signal conditions. This capacitance is exasperated with the PIN-NIP pair configuration since the diode area to ground is effectively doubled.

The Figure 2 PIN-NIP pair diode configuration was used to design both single and dual stage limiters over the 3 to 28 GHz frequency range. The PIN diode sizes were chosen before the design began in order to satisfy the power handling requirements of the limiters. In this case >6W (37.8dBm) operation was desired and therefore 35µm diodes were chosen from the survivability charts published in earlier work [6]. This is particularly important to consider for the first set of diodes in multiple stage designs. Experience has shown that these diodes are always the first to fail and therefore they should be sized appropriately to handle the MMIC's expected incident power.

The rest of the limiter design process was done from a small signal perspective after the initial consideration of diode size versus survivability was taken into consideration. This is very important since the size of the diodes dictate the amount of off-state shunting capacitance that occurs in the PIN-NIP pair because the largest capacitance, C_i , is dependent on diode area.

The limiter diode shunt capacitance is very effectively compensated by using it to create a Low Pass Filter (LPF) using standard filter design techniques [7]. The LPF structure is inherently broadband and can be designed to have excellent return loss characteristics and therefore low circuit insertion loss.

Figure 3 shows MMIC photos of the two limiters designed using this technique. Figure 3a is a single stage limiter that is effectively a 3 pole LPF (not considering both RF Bond Pad shunting capacitances). The dual stage limiter is simply a 5-pole filter. Both limiters started from lumped element Butterworth filter component values. The series inductances were realized by using high-Z, inductive microstrip lines. Initial distribution of the inductive elements used microstrip simulations, later the layout was EM simulated to fine tune the lengths and take into account mutual coupling between lines. Special attention was paid to minimizing the circuit die area for both circuits so that the GaAs cost could be kept to a minimum. The sizes of the MMICs are 0.907x0.866mm and 0.988x1.051mm for the single and dual stage limiters respectively. As expected, the higher complexity of the dual stage limiter drives the total die area, which is related to cost, up by 32%.



(a) (b)

Figure 3: MMIC VPIN Limiters

The LPF design approach works remarkably well and optimized quickly to the simulations shown in Figure 5 and 6. Both Limiters incorporated a series blocking capacitance on the input and output RF Bond Pads to protect the diodes from external biasing which can shift their limiting performance over input power. The series

capacitors create a Band Pass Filter (BPF) structure and cause the circuit to have high loss below 2GHz.

IV. Measured Results

Two GaAs VPIN wafers were fabricated and 6 limiter circuits of each type were randomly picked from each for fixturing and measurement. The fixtured die is soldered to Copper-Molly carrier plates for maximum heat conduction under large signal conditions. Two wire bonds are used to for the input and output RF bond pads as shown in the assembly diagram in Figure 5. The 10mil Alumina TFN microstrip were de-embedded during the measurements to the wire bond interconnections. The carriers were measured under ambient temperature conditions for all the measurements presented in this paper. In each graph all 12 limiters are displayed and illustrate the tightness of the performance distributions.

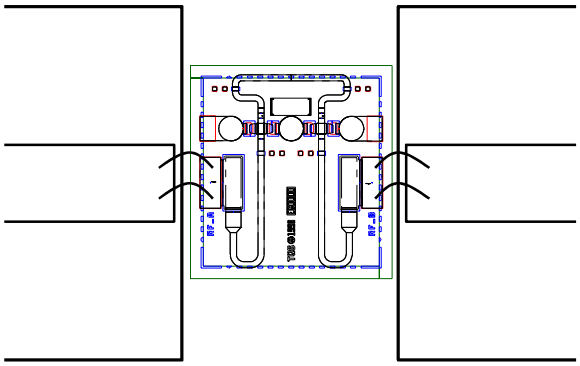


Figure 4: VPIN Limiter Assembly Diagram

The measured S-Parameter results for both limiters are shown in Figure 5 and 6. The small glitches in the performance are a result of the calibration and measurement system. The insertion loss for both limiters is extremely low and the designs came out reasonably close to small signal simulations. The limiters exhibit the classical BPF response with a drooping in the insertion loss caused by microstrip attenuation losses at the higher frequencies. The single stage limiter exhibits less than 0.39dB of insertion loss at the 10GHz while the dual stage limiter has 0.38dB of loss. Input and output reflection coefficients are typically better than 12dB across the band. The dual stage limiter had slightly better reflection loss over the bandwidth as would be expected from a higher order filter. The interesting comparison is that the dual stage limiter has better, or very comparable, performance to the single stage limiter over the 3 to 20GHz range. Above that the dual stage limiter has a couple tenths of dB extra insertion loss due to it having longer total microstrip length which causes more attenuation.

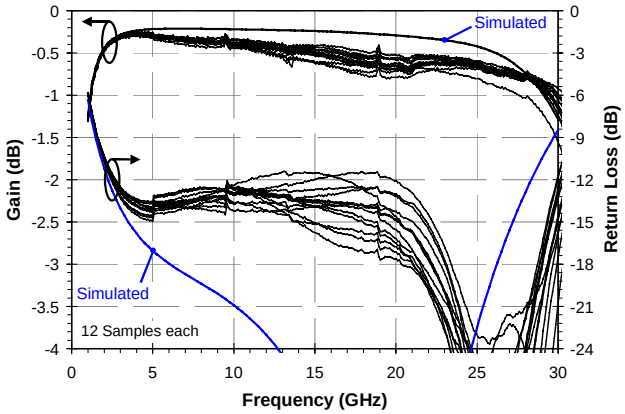


Figure 5: Single Stage VPIN Small Signal Performance

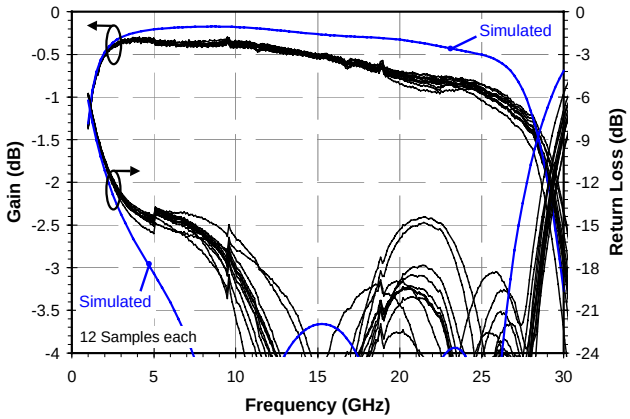


Figure 6: Dual Stage VPIN Small Signal Performance

The most interesting measurement comparison is of the sweeps over input power. The test set-up used a TWT to supply up to 36dBm of input power to the limiters. The 10GHz results are shown in Figure 7. This shows that the limiters have very low loss at small signal powers and then exhibit increasing attenuation, mostly from reflection, as input power is increased. The graphs illustrate three very critical points. First, there is no real "Flat Leakage" output power level for limiters. Their non-zero diode resistance always causes increasing output power as input power is increased. Limiters should therefore always be specified in terms of output power given a particular input power of RF system interest. It is also apparent that these two limiters compress very differently because one is a single stage and the other a dual stage limiter. The single stage limiter exhibits about 7 dB of attenuation at an input power of 28dBm. The dual stage limiter has 11dB of attenuation at the same 28dBm input power level. Clearly, the dual stage limiter is more desirable because it reflects more of the high input power wave without an increase in

small signal insertion loss. This is particularly important when considering the input power survivability of the following component, usually a low noise amplifier, is considered. An LNA's input P1dB Power may be as low as 18 to 20dBm depending on its input FET size.

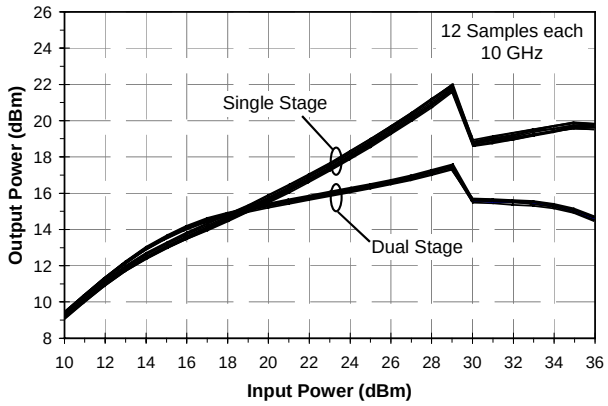


Figure 7: MMIC Limiter 10GHz Power Performance

The second interesting feature that Figure 8 illustrates is the "kink" in the output power. As shown, the effect is very real and repeatable from die to die. It is not a measurement system issue. The "kink" has been shown in many different PIN limiters and the root cause most commonly identified as being the second, or third, set of diodes moving significantly into forward conduction [7]. The measurements shown here are very important because both the single and dual stage limiters, containing the same size PIN-NIP pairs, exhibit the same exact kink location. These measurements confirm that the output power kink is independent on the number of PIN-NIP pairs and therefore is most probably the first set of diodes going into full forward conduction, or more exactly, having I-region punch through. A designer can take advantage of this phenomenon by achieving higher attenuation levels when the I-region punches through without harming the diodes.

The third interesting feature illustrated by Figure 8 is attenuation slope after the "kink". The single limiter continues to act as shunting low impedance by allowing the output power to linearly rise with increasing input power. The dual state limiter however provides additional varying attenuation as the second pair of diodes continues to change impedance. It is very likely that there will be another kink in the power sweep response at a little higher input power than was measured due to the I-region punch through for the second diodes.

V. Conclusions

Two limiters were designed with the same size PIN diodes in order to determine the size and performance trade-offs that would be made with the higher complexity dual stage limiter. The 10 GHz performance of each limiter is detailed in Table 1. Both limiters exhibit low loss and good Return Loss characteristics and can limit greater than 36dBm (4W) CW input power. Limiters have also been tested to survive up to 39dBm (8W) for short periods of time and even larger input powers under pulsed conditions. Table 1 demonstrates that the Dual Stage topology approach is the better limiter especially in the 3 to 20GHz range. This is except for the fact that the size of the dual stage limiter is about 32% larger due to the added complexity. The larger size, and increase cost, is perhaps a small consideration when the higher Input Power limiting performance is considered for sensitive components after the RP.

Table 1: VPIN Limiter Performance

10 GHz Performance	Single Stage	Dual Stage
Insertion Loss (dB)	< 0.39	< 0.38
Pout@Pin=28dBm (dBm)	21	17
Return Loss (dB)	>13	>18
CW Survivability (dBm)	>36	>36
Total Area (mm^2)	0.785	1.038

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